2114

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/084,105
Filed: February 27, 2002
Inventor(s):
Andrew Phelps

Title: A Memory Subsystem Including an Error Detection Mechanism for Address and Control Signals

§ § § § § § § § § § § § § § § § §

Examiner: Chu, Gabriel L.
Group/Art Unit: 2114
Atty. Dkt. No: 5181-97700

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Stephen J. Curran
Printed Name

Signature

3/21/05
Date

RESPONSE TO OFFICE ACTION OF MARCH 8, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Office Action of March 8, 2005, to further highlight why the application is in condition for allowance.